POINT NINE
Technologies, Inc.

# D2005 TetraFET

## 7.5W - 28V - 1GHz
## GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET

### FEATURES

- **METAL GATE**
- **EXTRA LOW Crss**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

### APPLICATIONS

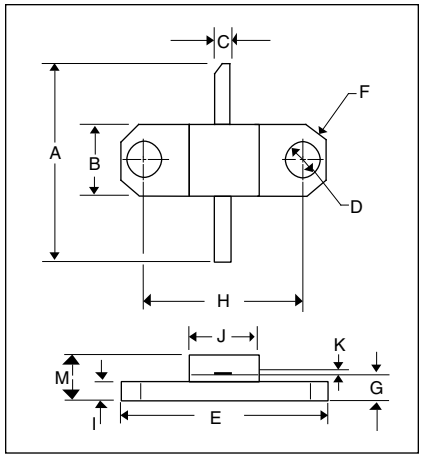
- **HF/VHF/UHF COMMUNICATIONS from DC to 1 GHz**

| ABSOLUTE MAXIMUM RATINGS ($T_{CASE}$ = 25°C unless otherwise stated) | | |
|---|---|---|
| $P_D$ | Power Dissipation | 35W |
| $BV_{DSS}$ | Drain-source breakdown voltage | 65V |
| $V_{GSS}$ | Gate-source voltage | ±20V |
| $I_D$ | Drain Current | 3A |
| $T_{stg}$ | Storage temperature | -65 to 150°C |
| $T_j$ | Maximum operating junction temperature | 200°C |
| $R_{THj\text{-}case}$ | Thermal resistance junction-case | Max. 5°C/W |

### ELECTRICAL CHARACTERISTICS ($T_{CASE}$ = 25°C unless otherwise stated)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Breakdown voltage, drain source | $V_{GS}$=0 $I_D$=10mA | 65 | | | Vdc |
| $I_{DSS}$ | Drain leakage current | $V_{DS}$=28V $V_{GS}$=0 | | | 0.6 | mAdc |
| $I_{GSS}$ | Gate leakage current | $V_{GS}$=20V $V_{DS}$=0 | | | 1 | µAdc |
| $V_{GS(th)}$ | Gate threshold voltage | $I_D$=10mA $V_{DS}$=$V_{GS}$ | 1 | | 7 | Vdc |
| gfs | Transconductance (300µs pulse) | $V_{DS}$=10V $I_D$=0.6A | 0.54 | | | Mhos |
| $G_{PS}$ | Common source power gain | $P_O$ =7.5W | 13 | | | dB |
| η | Drain efficiency | $V_{DS}$=28V $I_{DQ}$=0.6A | 50 | | | % |
| VSWR | Load mismatch tolerance | f=1GHz | 20:1 | | | |
| $C_{iss}$ | Input capacitance | $V_{DS}$=0V $V_{GS}$=-5V f=1MHz | | | 36 | pF |
| $C_{oss}$ | Output capacitance | $V_{DS}$=28V $V_{GS}$=0 f=1MHz | | | 18 | pF |
| $C_{rss}$ | Reverse transfer capacitance | $V_{DS}$=28V $V_{GS}$=0 f=1MHz | | | 1.5 | pF |

### DIMENSIONS




| DM | Millimeter | TOL | Inches | TOL |
|---|---|---|---|---|
| A | 16.51 | .25 | .650 | .010 |
| B | 6.35 | .13 | .250 | .005 |
| C | 1.52 | .13 | .060 | .005 |
| D | 3.30 | .13 | .130 | .005 |
| E | 18.92 | .05 | .745 | .002 |
| F | 1.27 X 45° | .13 | .030 X 45° | .005 |
| G | 2.16 | .13 | .085 | .005 |
| H | 14.22 | .05 | .560 | .002 |
| I | 1.52 | .13 | .060 | .005 |
| J | 6.35 | .13 | .250 | .005 |
| K | 0.10 | .02 | .004 | .001 |
| M | 5.08 | MAX | .200 | MAX |

**HAZARDOUS MATERIAL WARNING**

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

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*D2005

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D2005  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.4p
Lin    10    11    0.3n
Cin2   11    30    0.4p

LG    11    12    0.6n      ;Gate bond wire inductance
CGS   12    13    31.8p     ;Gate-source capacitance
MOS   14    12    13    13  D2005 L=0.9U W=0.0327    ;D G S B LEVEL1
JFET  16    13    14        D2005                    ;D G S
DBODY 13    16              D2005                    ;P N
LS    13    30    0.2n      ;Source bond wire inductance
CGD   12    16    0.9p      ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1  16    30    0.9p
Lout   16    20    0.5n
Cout2  20    30    0.65p

.MODEL D2005  NMOS (VTO=3.52 KP=7.77E-4 LAMBDA=0.0224 RD=0.2 RS=0.9)
.MODEL D2005  NJF  (VTO=-5.8 BETA=0.1098 LAMBDA=1.357)
.MODEL D2005  D    (CJO=45P RS=0.25 VJ=0.7 M=0.33 BV=70)

.ENDS
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