

5W - 28V - 1GHz
GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 2 GHz

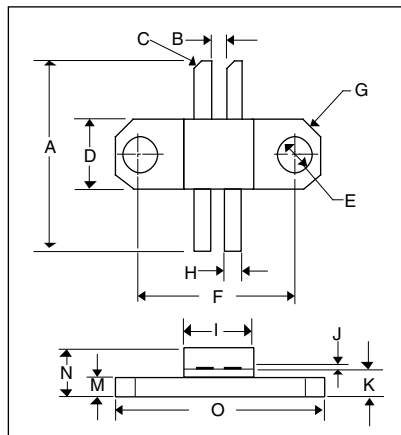
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	35W
BV_{DSS}	Drain-source breakdown voltage	65V
V_{GSS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	2A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 5.0°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<u>PER SIDE</u>					
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=10mA$	65			Vdc
I_{DSS}	Drain leakage current $V_{DS}=28V$ $V_{GS}=0$		0.2		mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$		1		μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
g_{fs}	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=.2A$	0.2			Mhos
<u>TOTAL DEVICE</u>					
G_{PS}	Common source power gain $P_O=5W$	13			dB
η	Drain efficiency $V_{DS}=28V$ $I_{DQ}=.4A$	40			%
VSWR	Load mismatch tolerance $f=1GHz$	20:1			
<u>PER SIDE</u>					
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			12	pF
C_{oss}	Output capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			6	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			0.5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	16.38	.26	.645	.010
B	1.52	.13	.060	.005
C	45°	5°	45°	5°
D	6.35	.13	.250	.005
E	3.30	.13	.130	.005
F	14.22	.13	.560	.005
G	x 45°	.13	.05 x 45°	.005
H	1.52	.13	.060	.005
I	6.35	.13	.250	.005
J	.13	.02	.005	.001
K	2.16	.13	.085	.005
M	1.52	.13	.060	.005
N	5.08	MAX	.200	MAX
O	18.90	5°	.744	.005

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

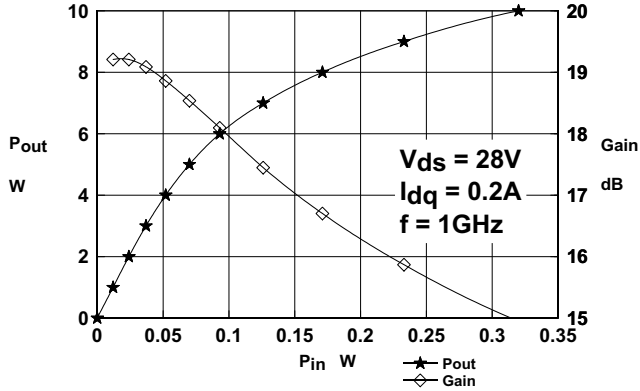


Figure 1 Output Power and Gain vs. Input power

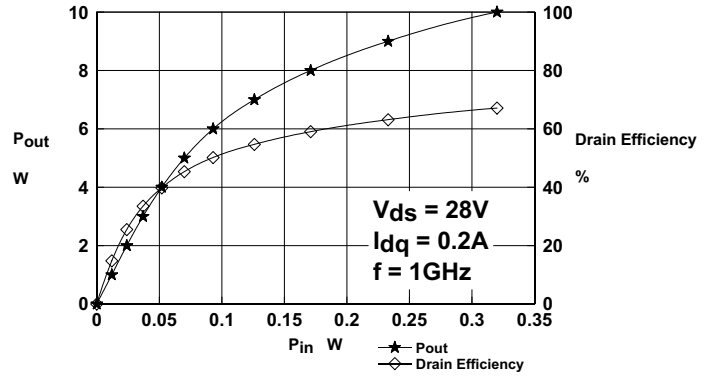


Figure 2 Output Power and Efficiency vs. Input Power

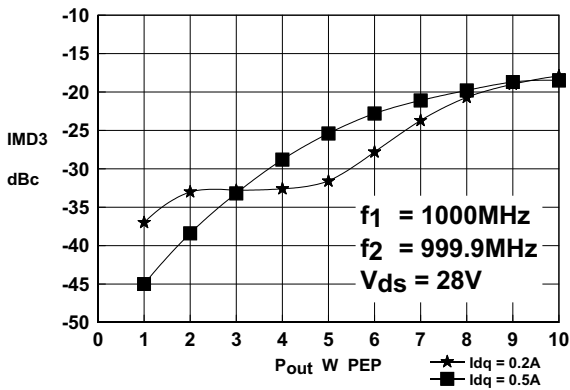


Figure 3 IMD Vs. Output Power.

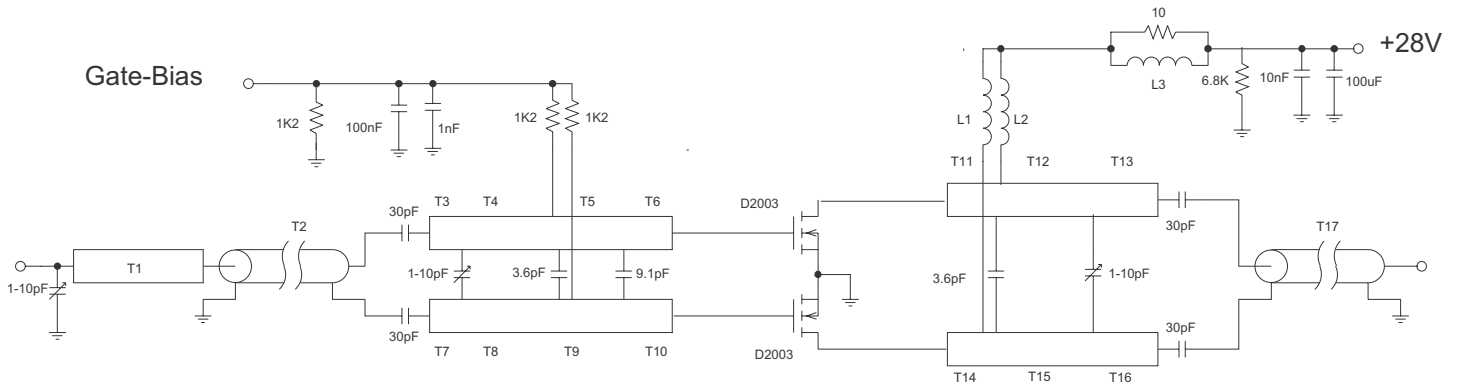
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z _S Ω	Z _L Ω
1000MHz	1.1 - j2.5	5.1 - j17.1

Typical S Parameters

! Vds=28V, Idq=0.1A
MHz S MA R 50

!Freq !MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
70	0.97	-36.4	15.8	156.6	0.017	67.2	0.91	-23.2
100	0.94	-48.0	14.1	146.3	0.021	58.1	0.88	-30.1
150	0.88	-65.3	12.3	129.9	0.027	45.5	0.81	-40.3
200	0.84	-78.5	10.2	114.7	0.029	34.8	0.77	-48.1
250	0.82	-88.4	8.8	106.0	0.029	28.1	0.75	-54.2
300	0.79	-97.1	7.7	98.3	0.029	27.3	0.73	-59.1
350	0.78	-105.5	6.9	88.5	0.028	22.2	0.72	-64.3
400	0.77	-113.3	6.0	84.5	0.026	24.2	0.71	-69.3
450	0.77	-121.8	5.4	77.8	0.024	23.3	0.70	-75.2
500	0.77	-128.9	4.9	75.3	0.022	29.6	0.70	-80.4
550	0.78	-136.7	4.6	68.3	0.020	35.0	0.70	-86.5
600	0.78	-144.0	4.4	65.4	0.020	46.6	0.70	-93.6
650	0.78	-150.8	4.0	57.2	0.020	57.6	0.70	-99.6
700	0.79	-156.7	3.7	52.3	0.022	68.5	0.71	-105.8
750	0.79	-160.9	3.4	46.7	0.025	76.6	0.70	-111.3
800	0.78	-164.2	3.0	41.4	0.028	81.6	0.69	-115.6
850	0.78	-166.3	2.7	39.5	0.032	87.8	0.68	-117.0
900	0.79	-168.5	2.6	38.4	0.036	92.3	0.68	-119.3
950	0.78	-170.3	2.5	36.8	0.044	97.4	0.70	-121.0
1000	0.79	-172.5	2.4	33.0	0.053	97.4	0.70	-124.2



1000MHz TEST FIXTURE

Substrate 0.8mm thick PTFE/glass
All microstrip lines $W = 2.7\text{mm}$

T1	15.7
T2, T17	45mm 50 OHM UT 34 semi-rigid coax
T3, T7	7mm
T4, T8	15mm
T5, T9	7.6mm
T6, T10	8mm
T11, T14	8mm
T12, T15	11.2mm
T13, T16	7mm
L1, L2	6 turns 24swg enamelled copper wire, 3mm i.d.
L3	1.5 turn 24swg enamelled copper wire on Siemens B62152-A7X 2 hole core

*D2003

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET

*May 2004

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*          _____GATE
*          I   _____DRAIN
*          I   I   _____SOURCE
*          I   I   I
.SUBCKT D2003  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1  10   30   0.38p
Lin   10   11   0.71n
Cin2  11   30   0.38p

LG    11   12   1n      ;Gate bond wire inductance
CGS   12   13   10.6p   ;Gate-source capacitance
MOS   14   12   13   13  D2003 L=0.9U W=0.0109   ;D G S B LEVEL1
JFET  16   13   14      D2003                   ;D G S
DBODY 13   16      D2003                   ;P N
LS    13   30   0.5n    ;Source bond wire inductance
CGD   12   16   0.3p    ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cin1  10   30   0.38p
Lin   10   11   0.71n
Cin2  11   30   0.38p

.MODEL D2003  NMOS (VTO=3.52 KP=7.77E-4 LAMBDA=0.0224 RD=0.6 RS=2.7)
.MODEL D2003  NJF  (VTO=-5.8 BETA=0.0366 LAMBDA=1.357)
.MODEL D2003  D    (CJO=15P RS=0.25 VJ=0.7 M=0.33 BV=70)

.ENDS
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