

60W - 12.5V - 175MHz
GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS

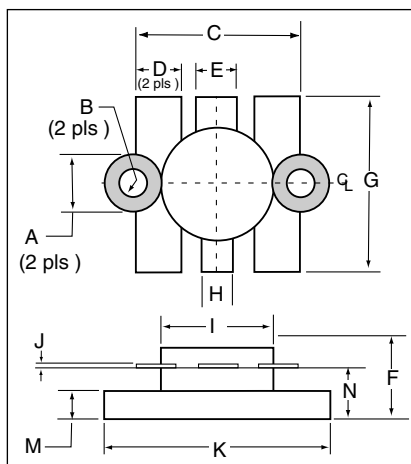
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	175W
BV_{DSS}	Drain-source breakdown voltage	40V
V_{GS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	40A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max.1.0°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	40			Vdc
I_{DSS}	Drain leakage current $V_{DS}=12.5V$ $V_{GS}=0$			4	mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$.5		7	Vdc
g_{fs}	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=4A$	3.2			mhos
G_{PS}	Common source power gain $P_O=50W$	10			dB
η	Drain efficiency $V_{DS}=12.5V$ $I_{DQ}=4A$	50			%
VSWR	Load mismatch tolerance $f=175MHz$	20:1			
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			240	pF
C_{oss}	Output capacitance $V_{DS}=12.5V$ $V_{GS}=0$ $f=1MHz$			180	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=12.5V$ $V_{GS}=0$ $f=1MHz$			16	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	6.35 DIA	.13	.250 DIA	.005
B	3.17 DIA	.13	.125 DIA	.005
C	18.41	.13	.725	.001
D	5.45	.13	.215	.005
E	5.21	.13	.205	.005
F	7.62	MAX	.300	MAX
G	21.59	.38	.850	.015
H	3.94	.13	.155	.005
I	4.32	.13	.170	.005
J	0.13	.02	.005	.001
K	24.76	.13	.975	.005
M	2.59	.13	.095	.005
N	4.06	.25	.170	.010

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

*D1260

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET

*May 2004

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*
*          _____GATE
*          I          _____DRAIN
*          I   I          _____SOURCE
*          I   I   I
.SUBCKT D1260 10 20 30
*Cin1,Cin2 & Lin model the input side of the package
Cin1 10 30 0.32p
Lin 10 11 0.59n
Cin2 11 30 0.32p

LG 11 12 2n ;Gate bond wire inductance
CGS 12 13 182.8p ;Gate-source capacitance
MOS 14 12 13 13 D1260 L=0.9U W=0.224 ;D G S B LEVEL1
JFET 16 13 14 D1260 ;D G S
DBODY 13 16 D1260 ;P N
LS 13 30 0.3n ;Source bond wire inductance
CGD 12 16 13.2p ;Gate-drain feedback capacitance
*Cut1,Cout2 & Lout model the output side of the package
Cout1 16 30 1.05p
Lout 16 20 1.77n
Cout2 20 30 1.05p

.MODEL D1260 NMOS (VTO=4.68 KP=2.687E-5 LAMBDA=0.01 RD=0.003 RS=0.09)
.MODEL D1260 NJF (VTO=-4.97 BETA=3.04 LAMBDA=3.385)
.MODEL D1260 D (CJO=552.4P RS=0.82 VJ=0.7 M=0.33 BV=50)

.ENDS
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