POINT NINE
Technologies, Inc.

D1207 TetraFET

20W - 12.5V - 500MHz
GOLD METALIZED MULTI-PURPOSE SILICON DMOS RF FET

FEATURES

- **METAL GATE**
- **EXTRA LOW Crss**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

APPLICATIONS

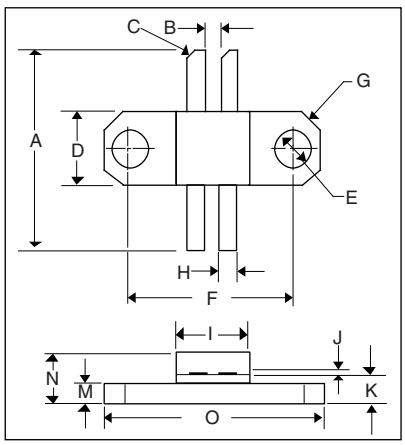
- **HF/VHF/UHF COMMUNICATIONS**

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C unless otherwise stated)		
P_D	Power Dissipation	100W
BV_{DSS}	Drain-source breakdown voltage	40V
V_{GSS}	Gate-source voltage	±20V
I_D	Drain Current	8A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj\text{-}case}$	Thermal resistance junction-case	Max. 1.75°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
		PER SIDE				
BV_{DSS}	Breakdown voltage, drain source	V_{GS}=0 I_D=100mA	40			Vdc
I_{DSS}	Drain leakage current	V_{DS}=12.5V V_{GS}=0			1	mAdc
I_{GSS}	Gate leakage current	V_{GS}=20V V_{DS}=0			1	µAdc
$V_{GS(th)}$	Gate threshold voltage	I_D=10mA V_{DS}=V_{GS}	0.5		7	Vdc
gfs	Transconductance (300µs pulse)	V_{DS}=10V I_D=1A	0.8			Mhos
		TOTAL DEVICE				
G_{PS}	Common source power gain	P_O=20W	10			dB
η	Drain efficiency	V_{DS}=12.5V I_{DQ}=0.8A	50			%
VSWR	Load mismatch tolerance	f=500MHz	20:1			
		PER SIDE				
C_{iss}	Input capacitance	V_{DS}=0V V_{GS}=-5V f=1MHz			60	pF
C_{oss}	Output capacitance	V_{DS}=12.5V V_{GS}=0 f=1MHz			40	pF
C_{rss}	Reverse transfer capacitance	V_{DS}=12.5V V_{GS}=0 f=1MHz			4	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	16.51	.26	.650	.010
B	1.52	.13	.060	.005
C	45°	5°	45°	5°
D	6.35	.13	.250	.005
E	3.30	.13	.130	.005
F	14.22	.13	.560	.005
G	1.27	.13	.05 x 45°	.005
H	1.52	.13	.060	.005
I	6.35	.13	.250	.005
J	.10	.03	.004	.001
K	2.16	.13	.085	.005
M	1.52	.13	.060	.005
N	5.08	MAX	.200	MAX
O	18.90	.13	.744	.005

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

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*D1207

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1207  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.38p
Lin    10    11    0.71n
Cin2   11    30    0.38p

LG    11    12    0.2n      ;Gate bond wire inductance
CGS   12    13    45.7p     ;Gate-source capacitance
MOS   14    12    13    13  D1207 L=0.9U W=0.056    ;D G S B LEVEL1
JFET  16    13    14        D1207                   ;D G S
DBODY 13    16              D1207                   ;P N
LS    13    30    0.3n      ;Source bond wire inductance
CGD   12    16    3.3p      ;Gate-drain feedback capacitance
*Cout1,Cout2 & Lout model the output side of the package
Cout1   16    30    0.38p
Lout    16    20    0.71n
Cout2   20    30    0.38p

.MODEL D1207  NMOS (VTO=4.68 KP=2.687E-5 LAMBDA=0.01 RD=0.012 RS=0.36)
.MODEL D1207  NJF  (VTO=-4.97 BETA=0.76 LAMBDA=3.385)
.MODEL D1207  D    (CJO=130.6P RS=0.82 VJ=0.7 M=0.35 BV=40)

.ENDS
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