

20W - 12.5V - 400MHz
GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 500MHz

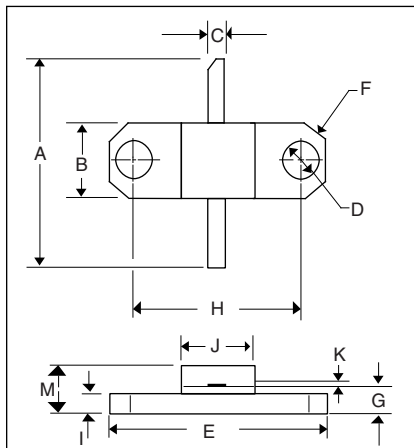
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	80W
BV_{DSS}	Drain-source breakdown voltage	40V
V_{GSS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	10A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 2.0°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	40			Vdc
I_{DSS}	Drain leakage current $V_{DS}=12.5V$ $V_{GS}=0$			4	mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$.5		5	Vdc
g_{fs}	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=2A$	1.6			Mhos
G_{PS}	Common source power gain $P_O=20W$	10			dB
η	Drain efficiency $V_{DS}=12.5V$ $I_{DQ}=2A$	50			%
VSWR	Load mismatch tolerance $f=400MHz$	20:1			
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			120	pF
C_{oss}	Output capacitance $V_{DS}=12.5V$ $V_{GS}=0$ $f=1MHz$			80	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=12.5V$ $V_{GS}=0$ $f=1MHz$			8.0	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	16.51	.25	.650	.010
B	6.35	.13	.250	.005
C	1.52	.13	.060	.005
D	3.30	.13	.130	.005
E	18.90	.05	.745	.005
F	1.27 X 45°	.13	.050 X 45°	.005
G	2.16	.13	.085	.005
H	14.22	.05	.560	.005
I	1.52	.13	.060	.005
J	6.35	.13	.250	.005
K	0.10	.02	.004	.001
M	5.08	MAX	.200	MAX

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

*D1202

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004

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*          -----GATE
*          I          -----DRAIN
*          I  I      -----SOURCE
*          I  I  I
.SUBCKT D1202 10 20 30
*Cin1,Cin2 & Lin model the input side of the package
Cin1 10 30 0.4p
Lin 10 11 0.3n
Cin2 11 30 0.4p
LG 11 12 0.7n ;Gate bond wire inductance
CGS 12 13 91.4p ;Gate-source capacitance
MOS 14 12 13 13 D1202 L=0.9U W=0.112 ;D G S B LEVEL1
JFET 16 13 14 D1202 ;D G S
DBODY 13 16 D1202 ;P N
LS 13 30 0.22n ;Source bond wire inductance
CGD 12 16 6.6p ;Gate-drain feedback capacitance
*Cout1,Cout2 & Lout model the output side of the package
Cout1 16 30 0.9p
Lout 16 20 0.5n
Cout2 20 30 0.65p

.MODEL D1202 NMOS (VTO=4.68 KP=2.687E-5 LAMBDA=0.01 RD=0.006 RS=0.18)
.MODEL D1202 NJF (VTO=-4.97 BETA=1.52 LAMBDA=3.385)
.MODEL D1202 D (CJO=261.2P RS=0.82 VJ=0.7 M=0.33 BV=50)

.ENDS
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