POINT NINE
Technologies, Inc.

# D1021 TetraFET

## *125W - 28V - 400MHz*
## GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET

### FEATURES

- **METAL GATE**
- **EXTRA LOW Crss**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

### APPLICATIONS

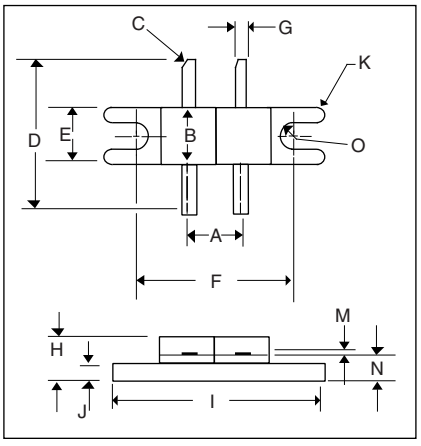
- **HF/VHF/UHF COMMUNICATIONS from DC to 400 MHz**

| ABSOLUTE MAXIMUM RATINGS ($T_{CASE}$ = 25°C unless otherwise stated) | | |
|---|---|---|
| $P_D$ | Power Dissipation | 350W |
| $BV_{DSS}$ | Drain-source breakdown voltage | 70V |
| $V_{GSS}$ | Gate-source voltage | ±20V |
| $I_D$ | Drain Current | 20A |
| $T_{stg}$ | Storage temperature | - 65 to 150°C |
| $T_j$ | Maximum operating junction temperature | 200°C |
| $R_{THj\text{-}case}$ | Thermal resistance junction-case | Max. 0.5°C/W |

### ELECTRICAL CHARACTERISTICS ($T_{CASE}$ = 25°C unless otherwise stated)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | PER SIDE | | | | |
| $BV_{DSS}$ | Breakdown voltage, drain source | $V_{GS}$=0 $I_D$=100mA | 70 | | | Vdc |
| $I_{DSS}$ | Drain leakage current | $V_{DS}$=28V $V_{GS}$=0 | | | 4 | mAdc |
| $I_{GSS}$ | Gate leakage current | $V_{GS}$=20V $V_{DS}$=0 | | | 1 | µAdc |
| $V_{GS(th)}$ | Gate threshold voltage | $I_D$=10mA $V_{DS}$=$V_{GS}$ | 1 | | 7 | Vdc |
| gfs | Transconductance (300µs pulse) | $V_{DS}$=10V $I_D$=4A | 3.2 | | | Mhos |
| | | TOTAL DEVICE | | | | |
| $G_{PS}$ | Common source power gain | $P_O$=125W | 13 | | | dB |
| η | Drain efficiency | $V_{DS}$=28V $I_{DQ}$=1.6A | 50 | | | % |
| VSWR | Load mismatch tolerance | f=400MHz | 20:1 | | | |
| | | PER SIDE | | | | |
| $C_{iss}$ | Input capacitance | $V_{DS}$=0V $V_{GS}$=-5V f=1MHz | | | 240 | pF |
| $C_{oss}$ | Output capacitance | $V_{DS}$=28V $V_{GS}$=0 f=1MHz | | | 120 | pF |
| $C_{rss}$ | Reverse transfer capacitance | $V_{DS}$=28V $V_{GS}$=0 f=1MHz | | | 10 | pF |

### DIMENSIONS




| DM | Millimeter | TOL | Inches | TOL |
|---|---|---|---|---|
| A | 6.45 | .13 | .254 | .005 |
| B | 6.35 | .13 | .250 | .005 |
| C | 45° | 5° | 45° | 5° |
| D | 16.51 | .76 | .650 | .030 |
| E | 6.48 | .13 | .255 | .005 |
| F | 18.42 | .13 | .725 | .005 |
| G | 1.52 | .13 | .060 | .005 |
| H | 4.06 | .25 | .160 | .010 |
| I | 24.77 | .13 | .975 | .005 |
| J | 1.52 | .13 | .060 | .001 |
| K | 0.81R | .13 | .032R | .005 |
| M | .010 | .03 | .004 | .001 |
| N | 2.16 | .13 | .085 | .005 |
| O | 1.65R | .03 | .065R | .005 |

**HAZARDOUS MATERIAL WARNING**

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

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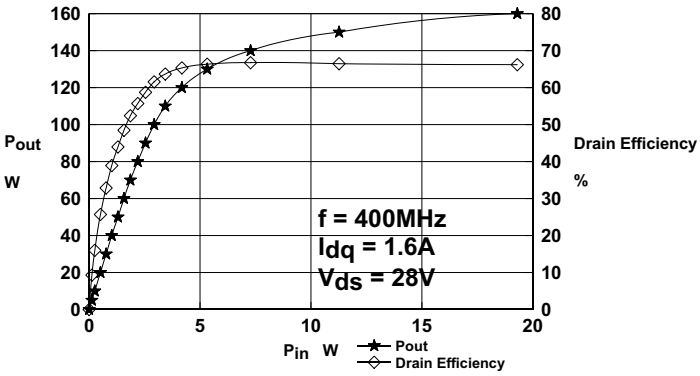


**Figure 1.**
Power Output and Efficiency vs. Input Power

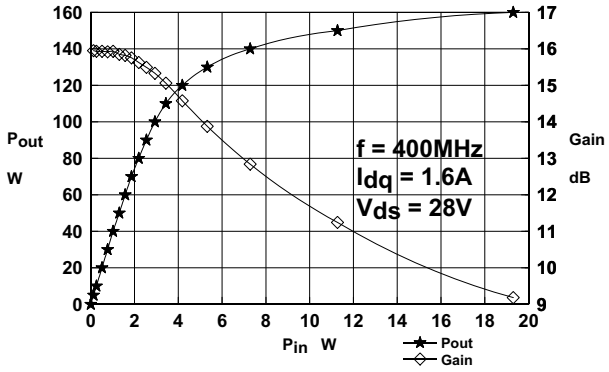


**Figure 2.**
Power Output and Gain vs. Input Power

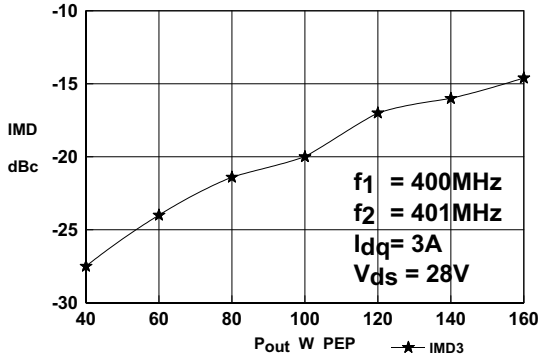


**Figure 3**
IMD vs.Power Output

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*D1021

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1021  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.4p
Lin    10    11    0.3n
Cin2   11    30    0.4p
LG     11    12    0.6n    ;Gate bond wire inductance
CGS    12    13    184p    ;Gate-source capacitance
MOS    14    12    13   13 D1021 L=0.9U W=0.224    ;D G S B LEVEL1
JFET   16    13    14      D1021                      ;D G S
DBODY  13    16            D1021                      ;P N
LS     13    30    0.2n    ;Source bond wire inductance
CGD    12    16    4p      ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1   16    30    0.9p
Lout    16    20    0.5n
Cout2   20    30    0.65p

.MODEL D1021  NMOS (VTO=4.76 KP=2.81E-5 LAMBDA=0.032 RD=0.019 RS=0.077)
.MODEL D1021  NJF  (VTO=-4.3 BETA=1 LAMBDA=0.54)
.MODEL D1021  D    (CJO=328.8P RS=0.25 VJ=0.7 M=0.35 BV=75)

.ENDS
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