

100W - 28V - 500MHz
GOLD METALIZED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 500MHz

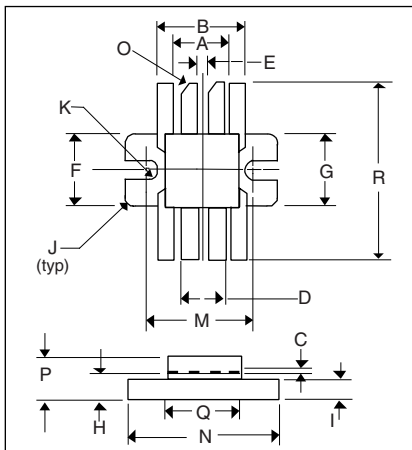
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	250W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	15A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 0.7°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<u>PER SIDE</u>					
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	70			Vdc
I_{DSS}	Drain leakage current $V_{DS}=28V$ $V_{GS}=0$			3	mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
gfs	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=3A$	2.4			Mhos
<u>TOTAL DEVICE</u>					
G_{PS}	Common source power gain $P_o=100W$	10			dB
η	Drain efficiency $V_{DS}=28V$ $I_{DQ}=1.2A$	50			%
VSWR	Load mismatch tolerance $f=500MHz$	20:1			
<u>PER SIDE</u>					
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			180	pF
C_{oss}	Output capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			90	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			7.5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	9.14	.13	.360	.005
B	12.70	.13	.500	.005
C	0.13	.03	.005	.001
D	6.86	.13	.270	.005
E	0.76	.13	.030	.005
F	9.78	.13	.385	.005
G	10.16	.13	.400	.005
H	4.19	.13	.165	.005
I	3.18	.13	.125	.005
J	1.52R	.13	.060R	.005
K	1.65R	.13	.065R	.005
M	16.51	.13	.650	.005
N	22.86	.13	.900	.005
O	45°	5°	45°	5°
P	6.35	.64	.250	.025
Q	10.77	.13	.424	.005
R	19.05	.25	.750	.010

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

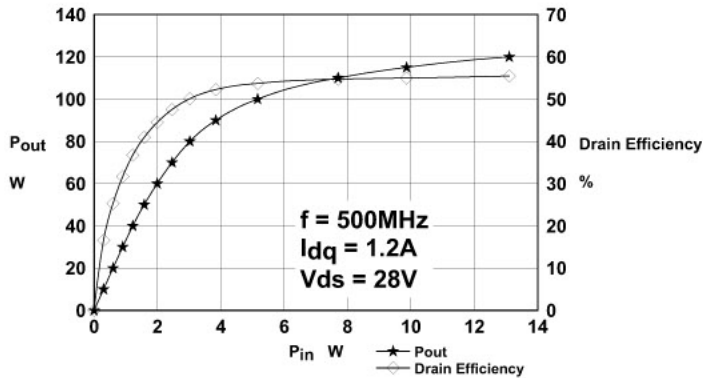


Figure 1

Power Output and Efficiency vs Input Power

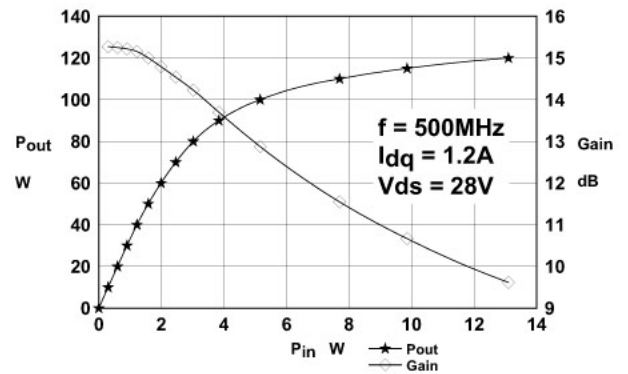


Figure 2

Power Output and Gain vs Input Power

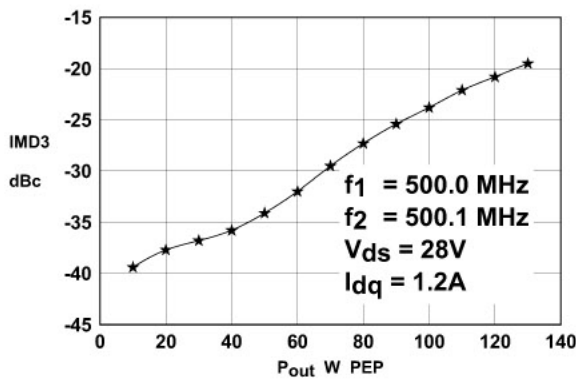


Figure 3

IMD vs. Output Power

OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
500	2.0 - j2.2	2.6 - j0.6

N.B. Impedances measured terminal to terminal

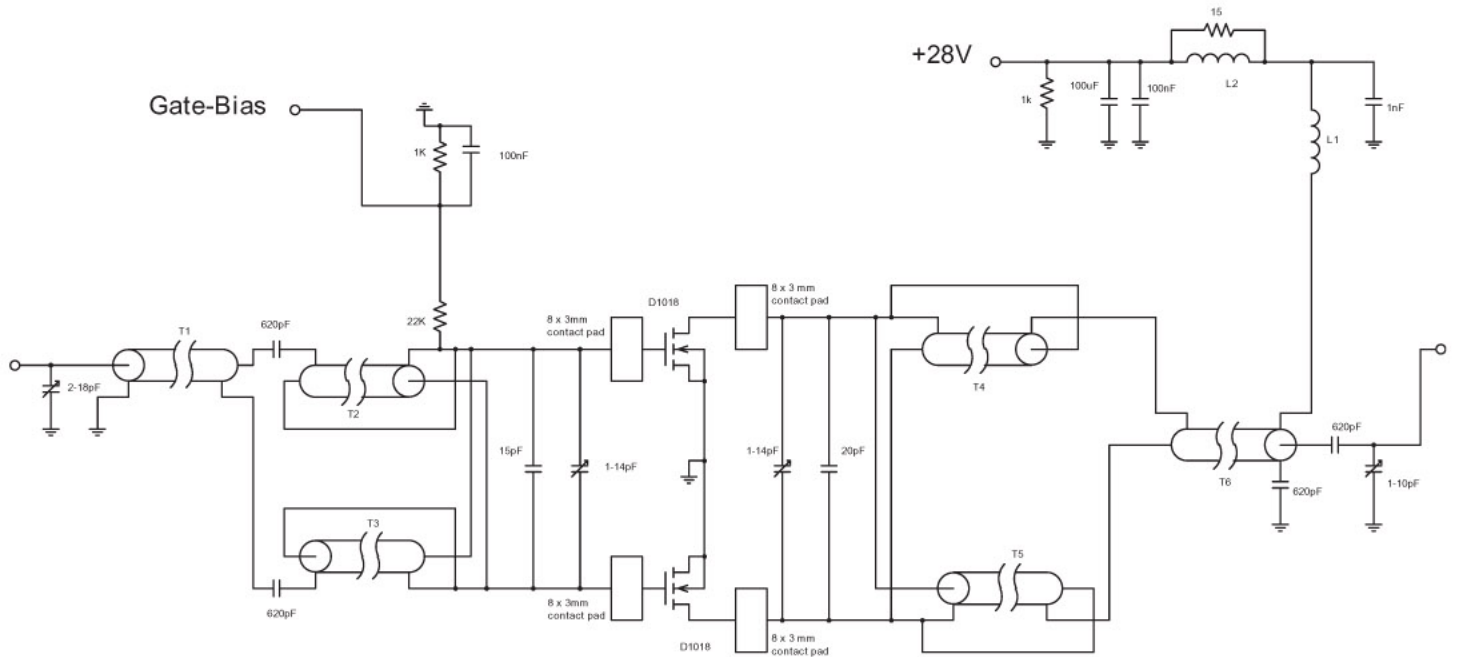
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Typical S Parameters

! Vds=28V, Idq=0.3A
MHZ S MA R 50

!Freq !MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
100	0.86	-157.3	5.98	55.7	0.01	20.3	0.73	-139.7
150	0.9	-163.2	3.22	43.1	0.01	78	0.82	-149.7
200	0.93	-167.9	1.98	36.9	0.02	98.2	0.88	-156.3
250	0.95	-170.4	1.39	31	0.03	101	0.91	-160.2
300	0.95	-172.7	1.1	29.6	0.05	103.7	0.93	-163.6
350	0.96	-174.5	0.82	23.9	0.06	99.9	0.94	-166.1
400	0.96	-176.2	0.69	23.9	0.08	100.2	0.95	-168.1
450	0.97	-177.5	0.55	22.1	0.09	98.3	0.96	-170.1
500	0.97	-179.4	0.51	21	0.11	95.6	0.97	-171.6
550	0.97	179.8	0.43	19.1	0.13	90.8	0.97	-173.3
600	0.96	178.8	0.4	15.1	0.15	82	0.97	-174.5
650	0.98	177.5	0.35	15.8	0.17	83.5	0.98	-175.7
700	0.99	175.4	0.31	11	0.19	76.8	1	-178.4
750	0.99	173	0.27	14.2	0.21	75.1	1.01	178.8
800	1	170.5	0.24	16.6	0.22	71.5	1	176.1
850	0.99	168.1	0.24	22.7	0.25	72.6	0.99	173.3
900	1	166.1	0.24	23.7	0.3	68.8	0.99	170.6
950	1	163.9	0.25	23.2	0.34	62.7	0.97	167.7
1000	0.99	161.6	0.25	21.7	0.37	56.4	0.96	166.1

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500MHz TEST FIXTURE

- T1,6** 65mm 50ohm UT85 semi-rigid coax
- T2,3,4,5** 75mm 15 ohm UT85-15 semi-rigid coax
- L1** 6 turns 21 swg enamelled copper wire, 3mm id.
- L2** 8.5 turns 19swg enamelled copper wire on Fair-Rite FT82-43 core
- T6** Placed through Ferronics 12-360-K ferrite bead

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*D1018

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET

*May 2004

```
*          _____GATE
*          I   _____DRAIN
*          I   I   _____SOURCE
*          I   I   I
.SUBCKT D1018  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1  10   30   0.47p
Lin   10   11   0.67n
Cin2  11   30   0.47p
LG    11   12   0.6n           ;Gate bond wire inductance
CGS   12   13   138p          ;Gate-source capacitance
MOS   14   12   13   13   D1018 L=0.9U W=0.168           ;D G S B LEVEL1
JFET  16   13   14           D1018                       ;D G S
DBODY 13   16           D1018                       ;P N
LS    13   30   0.3n         ;Source bond wire inductance
CGD   12   16   3p           ;Gate-drain feedback capacitance
*Cout1,Cout2 & Lout model the output side of the package

Cout1 16   30   0.77p
Lout   16   20   1.19n
Cout2 20   30   0.70p

.MODEL D1018 NMOS (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.025 RS=0.102)
.MODEL D1018 NJF (VTO=-4.3 BETA=0.75 LAMBDA=0.54)
.MODEL D1018 D (CJO=246.6P RS=0.25 VJ=0.7 M=0.35 BV=75)

.ENDS
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