POINT NINE
Technologies, Inc.

D1012 TetraFET

100W - 28V - 500MHz

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET

FEATURES

- **METAL GATE**
- **EXTRA LOW C_{rss}**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

APPLICATIONS

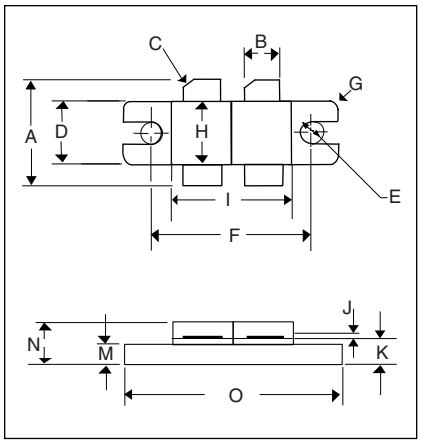
- **HF/VHF/UHF COMMUNICATIONS from DC to 500 MHz**

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C unless otherwise stated)		
P_D	Power Dissipation	290W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	±20V
I_D	Drain Current	15A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 0.6°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
		PER SIDE					
BV_{DSS}	Breakdown voltage, drain source	V_{GS}=0	I_D=100mA	70			Vdc
I_{DSS}	Drain leakage current	V_{DS}=28V	V_{GS}=0			3	mAdc
I_{GSS}	Gate leakage current	V_{GS}=20V	V_{DS}=0			1	µAdc
$V_{GS(th)}$	Gate threshold voltage	I_D=10mA	V_{DS}=V_{GS}	1		7	Vdc
gfs	Transconductance (300µs pulse)	V_{DS}=10V	I_D=3A	2.4			Mhos
		TOTAL DEVICE					
G_{PS}	Common source power gain	P_O=100W		10			dB
η	Drain efficiency	V_{DS}=28V	I_{DQ}=1.2A	50			%
VSWR	Load mismatch tolerance	f=500MHz		20:1			
		PER SIDE					
C_{iss}	Input capacitance	V_{DS}=0V	V_{GS}=-5V f=1MHz			180	pF
C_{oss}	Output capacitance	V_{DS}=28V	V_{GS}=0 f=1MHz			90	pF
C_{rss}	Reverse transfer capacitance	V_{DS}=28V	V_{GS}=0 f=1MHz			7.5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	13.7	MIN	.54	MIN
B	5.72	.13	.225	.005
C	45°	5°	45°	5°
D	9.78	.13	.385	.005
E	1.65R	.13	.065R	.005
F	23.75	.13	.935	.005
G	1.52R	.13	.060R	.005
H	9.53	.13	.375	.005
I	19.18	.26	.755	.010
J	.13	.02	.005	.001
K	2.54	.13	.100	.005
M	1.52	.13	.060	.005
N	4.57	.50	.180	.020
O	30.48	.13	1.200	.005

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

2697 Lavery Court #8 • Newbury Park, CA 91320 • (805) 375-6600 • Fax: (805) 375-6602 • www.point9.com • www.rfmosfet.com

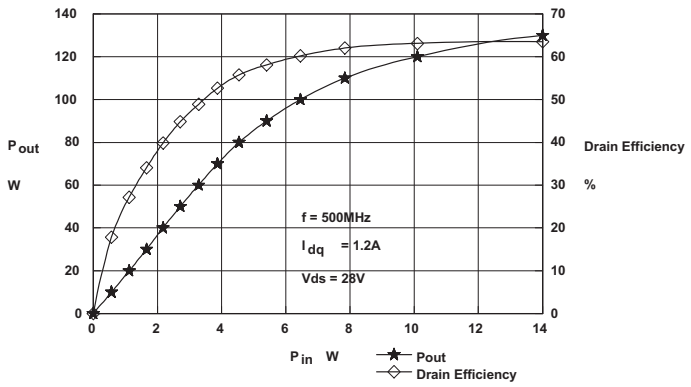


Figure 1 - Power Output and Efficiency vs. Power Input.

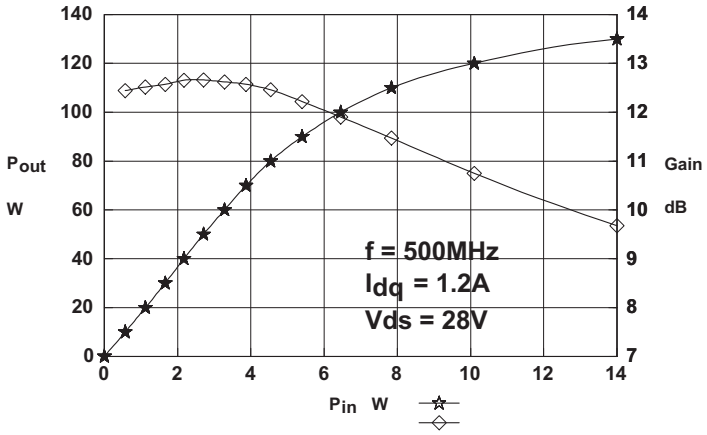


Figure 2 - Power Output & Gain vs. Power Input.

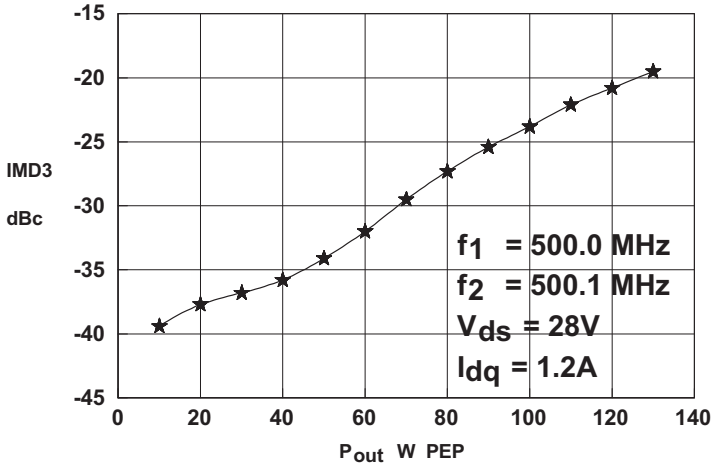
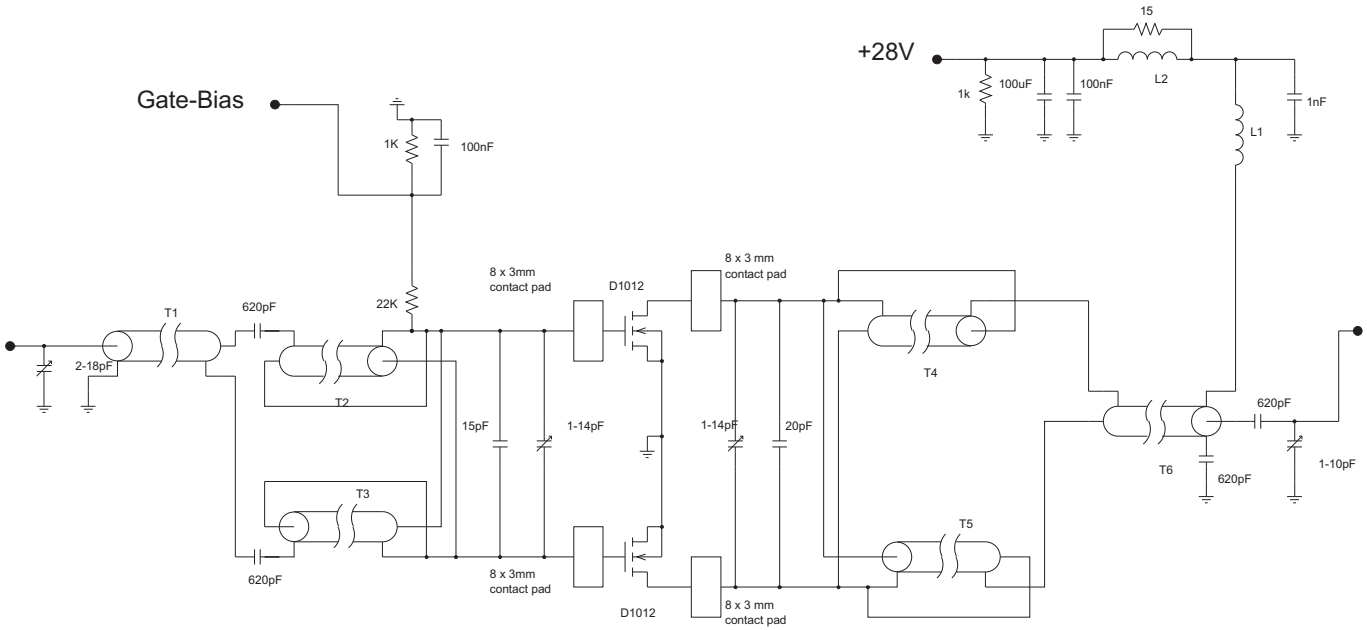


Figure 3 - IMD vs. Output Power.

D1012
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
500	2.0 - j2.2	2.6 - j0.6

N.B. Impedances measured terminal to terminal



D1012 500MHz TEST FIXTURE

T1,6	65mm	50 Ohm UT85 semi-rigid coax
T2,3,4,5	75mm	15 Ohm UT85-15 semi-rigid coax
L1	6 turns	21 swg enamelled copper wire, 3mm i.d.
L2	8.5 turns	19 swg enamelled copper wire on Fair-Rite FT82-43 core

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*D1012

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1012  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.51p
Lin    10    11    0.44n
Cin2   11    30    0.51p
LG     11    12    0.6n       ;Gate bond wire inductance
CGS    12    13    138p       ;Gate-source capacitance
MOS    14    12    13     13  D1012 L=0.9U W=0.168    ;D G S B LEVEL1

JFET   16    13    14    D1012                        ;D G S
DBODY  13    16    D1012                              ;P N
LS     13    30    0.25n      ;Source bond wire inductance
CGD    12    16    3p         ;Gate-drain feedback capacitance
*Cout1,Cout2 & Lout model the output side of the package
Cout1  16    30    1p
Lout   16    20    0.85n
Cout2  20    30    1p

.MODEL D1012 NMOS (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.025
 RS=0.102)
.MODEL D1012  NJF  (VTO=-4.3 BETA=0.75 LAMBDA=0.54)
.MODEL D1012  D    (CJO=246.6P RS=0.25 VJ=0.7 M=0.35 BV=75)

.ENDS
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