

**150W - 28V - 500MHz**  
**GOLD METALLISED MULTI-PURPOSE**  
**SILICON DMOS RF FET**

**FEATURES**

- METAL GATE
- EXTRA LOW  $C_{rss}$
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

**APPLICATIONS**

- HF/VHF/UHF COMMUNICATIONS  
from DC to 500 MHz

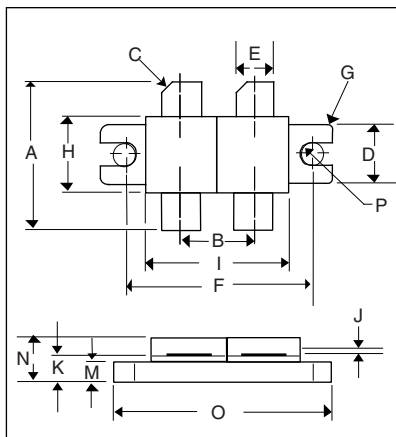
**ABSOLUTE MAXIMUM RATINGS**  
( $T_{CASE} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	389W
$BV_{DSS}$	Drain-source breakdown voltage	70V
$V_{GS}$	Gate-source voltage	$\pm 20V$
$I_D$	Drain Current	20A
$T_{stg}$	Storage temperature	65 to 150°C
$T_j$	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 0.45°C/W

**ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^{\circ}C$  unless otherwise stated)**

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<u>PER SIDE</u>					
$BV_{DSS}$	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	70			Vdc
$I_{DSS}$	Drain leakage current $V_{DS}=28V$ $V_{GS}=0$			4	mAdc
$I_{GSS}$	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	$\mu$ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
$g_{fs}$	Transconductance (300 $\mu$ s pulse) $V_{DS}=10V$ $I_D=4A$	3.2			Mhos
<u>TOTAL DEVICE</u>					
$G_{ps}$	Common source power gain $P_O=150W$	10			dB
$\eta$	Drain efficiency $V_{DS}=28V$ $I_{DQ}=2A$	60			%
VSWR	Load mismatch tolerance $f=500MHz$	20:1			
<u>PER SIDE</u>					
$C_{iss}$	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			240	pF
$C_{oss}$	Output capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			100	pF
$C_{rss}$	Reverse transfer capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			10	pF

**DIMENSIONS**

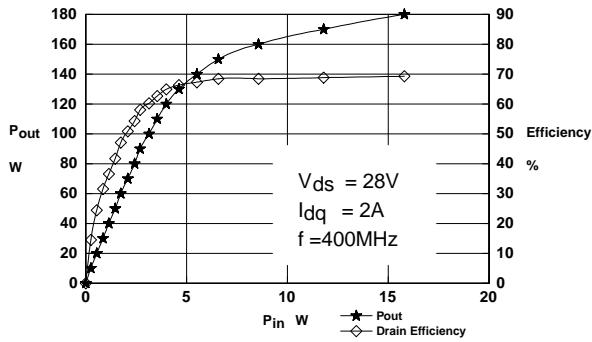


DM	Millimeter	TOL	Inches	TOL
A	19.05	.50	.750	.020
B	10.9	.25	.430	.010
C	45°	.05	45°	5°
D	9.78	.13	.385	.005
E	5.71	.13	.225	.005
F	27.94	.13	1.100	.005
G	1.52R	.13	.060R	.005
H	10.16	.13	.400	.005
I	22.22	MAX	.875	MAX
J	0.13	.02	.005	.001
K	2.72	.13	.107	.005
M	1.65	.13	.065	.005
N	5.08	.50	.200	.020
O	34.04	.13	1.340	.005
P	1.65R	.13	.065R	.005

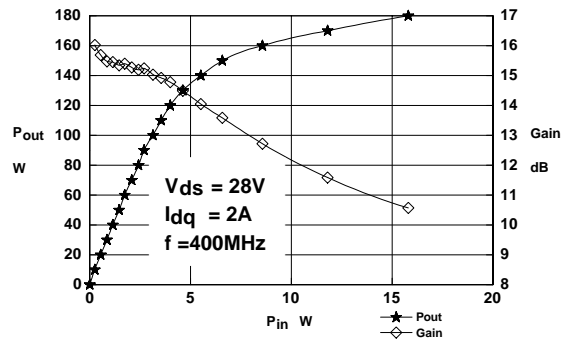
**HAZARDOUS MATERIAL WARNING**

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

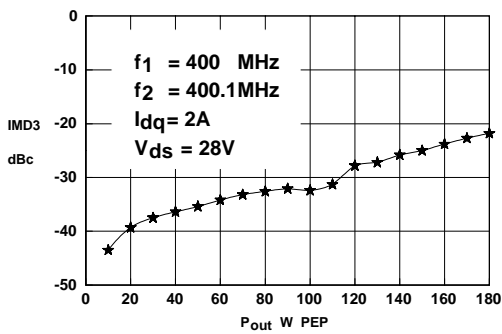
U.S. PATENTS 5,121,176 & 5,179,032  
GLOBAL PATENTS PENDING



**Figure 1 – Power Output and Efficiency vs. Power Input.**



**Figure 2 – Power Output & Gain vs. Power Input.**



**Figure 3 – IMD vs. Output Power.**

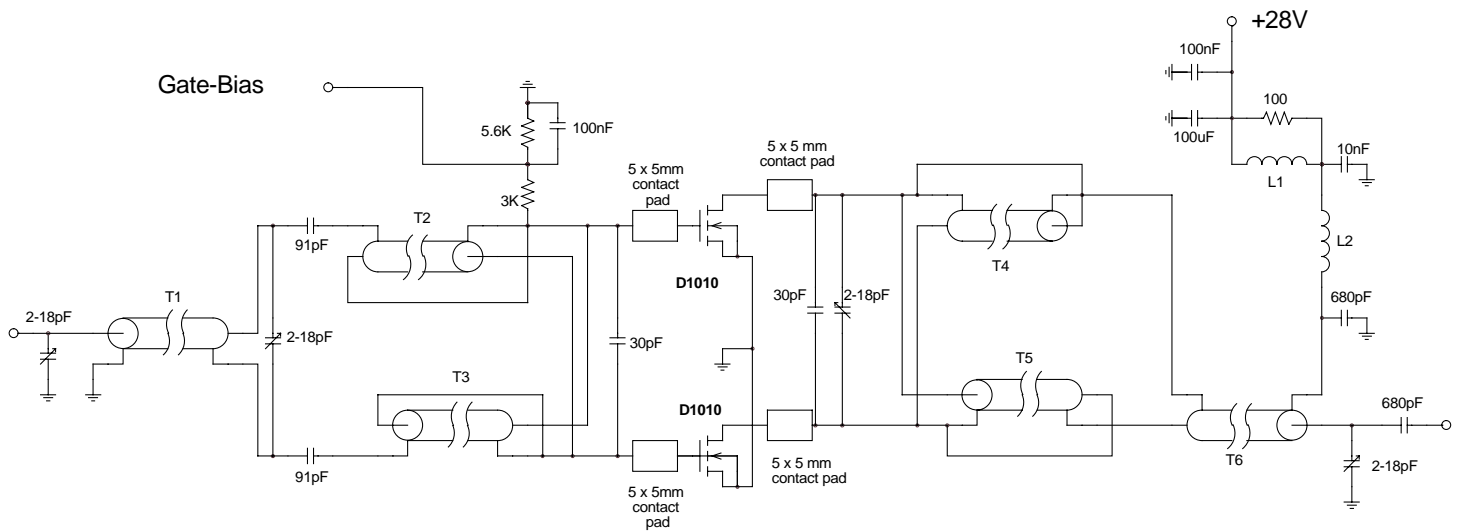
**D1010  
OPTIMUM SOURCE AND LOAD IMPEDANCE**

Frequency MHz	$Z_S$ $\Omega$	$Z_L$ $\Omega$
400	$1.7 + j0.1$	$2.7 + j1$

**Typical S Parameters**

! Vds=28V Idq=1A per side  
# MHZ S MA R 50

!Freq !MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
20	0.729	-173.6	20.47	103.6	0.011	25	0.557	-172.3
30	0.72	-172.9	20.57	97.4	0.012	13.7	0.5664	-169.2
40	0.725	-171.7	18.45	91.1	0.012	7.4	0.5848	-167.8
50	0.745	-171.5	14.74	85.1	0.011	3.1	0.6097	-165.5
60	0.758	-170.7	12.21	79.6	0.011	0.7	0.6365	-164.4
70	0.773	-171	10.35	75.6	0.01	-1.1	0.6634	-163.7
80	0.794	-170.6	8.943	70.5	0.01	-2.4	0.6935	-163.8
90	0.81	-170.6	7.829	65.7	0.009	-3.2	0.712	-164
100	0.831	-170.9	6.878	61.9	0.009	-2.6	0.734	-163.6
110	0.841	-171.4	6.107	58.6	0.008	-2.4	0.7559	-164
120	0.852	-171.8	5.449	54.9	0.007	-1	0.7685	-164.8
130	0.862	-172.1	4.877	52.4	0.007	1.9	0.7902	-165.2
140	0.871	-172.6	4.373	48.8	0.006	4.8	0.8089	-166
150	0.885	-173.1	3.949	46.1	0.006	8.8	0.8248	-165.9
160	0.895	-173.5	3.574	42.4	0.006	13.8	0.8333	-166.9
170	0.901	-174.1	3.246	40.4	0.005	19.7	0.8413	-167.7
180	0.905	-175.2	2.948	38.5	0.005	26.8	0.8512	-168.5
190	0.911	-175	2.688	36.6	0.005	35.5	0.8696	-168.5
200	0.915	-175.8	2.486	36	0.005	42.5	0.871	-169.4
210	0.922	-175.8	2.313	35	0.006	50.3	0.8817	-169.4
220	0.933	-176.4	2.16	33.7	0.006	56.4	0.8865	-170.3
230	0.927	-176.4	2.013	31.9	0.006	60.1	0.8966	-171
240	0.93	-177.3	1.866	29.5	0.007	62.9	0.8999	-171.5
250	0.938	-177.2	1.729	27.4	0.007	66.7	0.9096	-171.4
260	0.939	-178.4	1.617	26.1	0.008	70.8	0.9101	-172.3
270	0.94	-178.6	1.502	24.8	0.008	73.5	0.9152	-172.5
280	0.942	-179	1.433	24.5	0.009	76.7	0.9159	-173
290	0.95	-179.9	1.359	25.1	0.01	80.4	0.923	-173.6
300	0.944	-179.3	1.3	24.1	0.011	81.3	0.9216	-173.9
310	0.951	-179.5	1.238	22.3	0.012	81.5	0.9297	-174.8
320	0.952	179.6	1.184	20.4	0.012	80.4	0.9345	-174.8
330	0.954	-179.9	1.115	18.3	0.013	79	0.9344	-175.4
340	0.963	179.2	1.04	15.7	0.013	77.5	0.9394	-175.6
350	0.953	178.9	0.964	13.8	0.014	77.5	0.9382	-176.2
360	0.96	178.3	0.9	13	0.014	78.1	0.943	-176.2
370	0.96	178.4	0.847	13.1	0.015	78.6	0.9437	-176.8
380	0.96	177.7	0.802	13.1	0.015	79.6	0.9458	-176.9
390	0.963	177.5	0.744	12.6	0.015	78.6	0.9475	-177.2
400	0.964	177	0.704	16.9	0.015	82.9	0.9492	-177.5
410	0.966	176.5	0.721	16.3	0.017	84	0.9527	-177.3
420	0.964	176.8	0.704	14.6	0.018	83.1	0.9499	-178.2
430	0.965	176.5	0.677	12.1	0.018	81.8	0.9556	-178.2
440	0.965	175.6	0.64	10.3	0.019	80.5	0.9593	-178.8
450	0.967	175.3	0.605	9.7	0.019	81	0.9546	-179
460	0.968	175.1	0.576	8.8	0.019	81.2	0.9598	-179.7
470	0.967	175.2	0.552	9.4	0.02	82.4	0.9599	-179.4
480	0.966	174.8	0.53	9.7	0.02	83.6	0.9608	-179.9
490	0.967	174.3	0.512	9.4	0.021	83.2	0.9604	179.8
500	0.967	173.9	0.503	9.5	0.022	83.8	0.9596	179.5



## D1010 TEST FIXTURE

Substrate 1.6mm PTFE/ glass,  $\epsilon_r = 2.5$   
All microstrip lines  $W = 4.4\text{mm}$

T1	12cm	50 $\Omega$ UT85 semi-rigid coax on ferrite core
T2,3	7.5cm	15 $\Omega$ UT85-15 semi-rigid coax
T4,5	7cm	15 $\Omega$ UT85-15 semi-rigid coax
T6	11cm	50 $\Omega$ UT85 semi-rigid coax on ferrite core
L1	6.5 turns	25swg enamelled copper wire on Fair-Rite FT50B-43 core
L2	6.5 turns	25swg enamelled copper wire, 4mm internal diameter

\*D1010

\*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET

\*May 2004

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*          _____GATE
*          I   _____DRAIN
*          I   I   _____SOURCE
*          I   I   I
.SUBCKT D1010  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1  10   30   0.79p
Lin   10   11   0.38n
Cin2  11   30   0.79p
LG    11   12   0.6n           ;Gate bond wire inductance
CGS   12   13   184p          ;Gate-source capacitance
MOS   14   12   13   13  D1010 L=0.9U W=0.224      ;D G S B
LEVEL1
JFET  16   13   14           D1010                ;D G S
DBODY 13   16           D1010                ;P N
LS    13   30   0.2n         ;Source bond wire inductance
CGD   12   16   4p           ;Gate-drain feedback capacitance
*Cout1,Cout2 & Lout model the output side of the package
Cout1 16   30   1.38p
Lout   16   20   0.73n
Cout2  20   30   1.15p

.MODEL D1010 NMOS (VTO=4.76 KP=2.81E-5 LAMBDA=0.032 RD=0.019 RS=0.077)
.MODEL D1010 NJF (VTO=-4.3 BETA=1 LAMBDA=0.54)
.MODEL D1010 D (CJO=328.8P RS=0.25 VJ=0.7 M=0.35 BV=75)

.ENDS
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