

20W - 28V - 500MHz

**GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET**

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 850 MHz

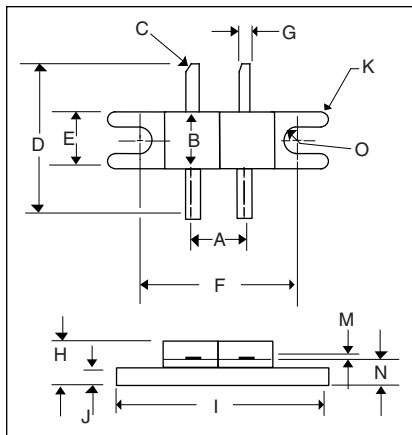
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	100W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	5A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 1.75°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PER SIDE					
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	70			Vdc
I_{DSS}	Drain leakage current $V_{DS}=28V$ $V_{GS}=0$			1	mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
g_{fs}	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=1A$	0.8			Mhos
TOTAL DEVICE					
G_{ps}	Common source power gain $P_o=20W$	13			dB
η	Drain efficiency $V_{DS}=28V$ $I_{DQ}=0.4A$	50			%
VSWR	Load mismatch tolerance $f=500MHz$	20:1			
PER SIDE					
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			60	pF
C_{oss}	Output capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			30	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			2.5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	6.45	.13	.254	.005
B	6.35	.13	.250	.005
C	45°	5°	45°	5°
D	16.51	.76	.650	.030
E	6.48	.13	.255	.005
F	18.42	.13	.725	.005
G	1.52	.13	.060	.005
H	4.06	.25	.160	.010
I	24.77	.13	.975	.005
J	1.52	.13	.060	.001
K	0.81R	.13	.032R	.005
M	.010	.03	.004	.001
N	2.16	.13	.085	.005
O	1.65R	.03	.065R	.005

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

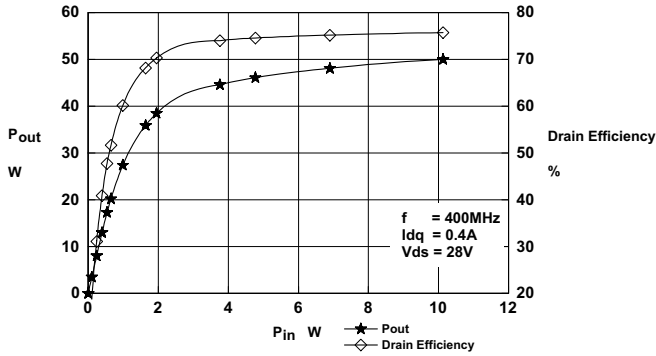


Figure 1

Power Output and efficiency vs. Power Input.

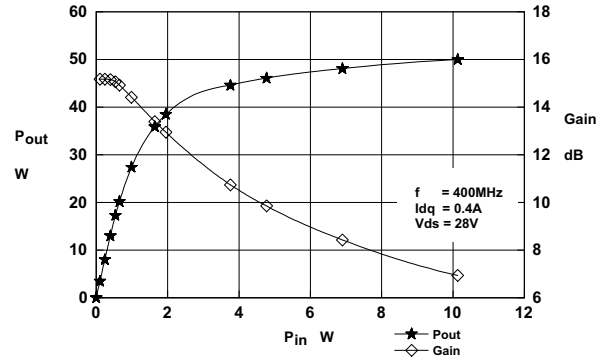


Figure 2

Power Output and Gain vs. Power Input.

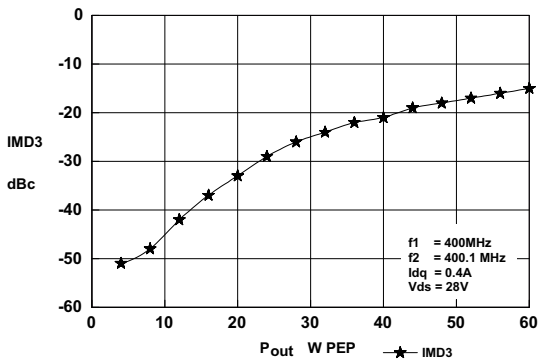


Figure 3

IMD Vs. Output Power.

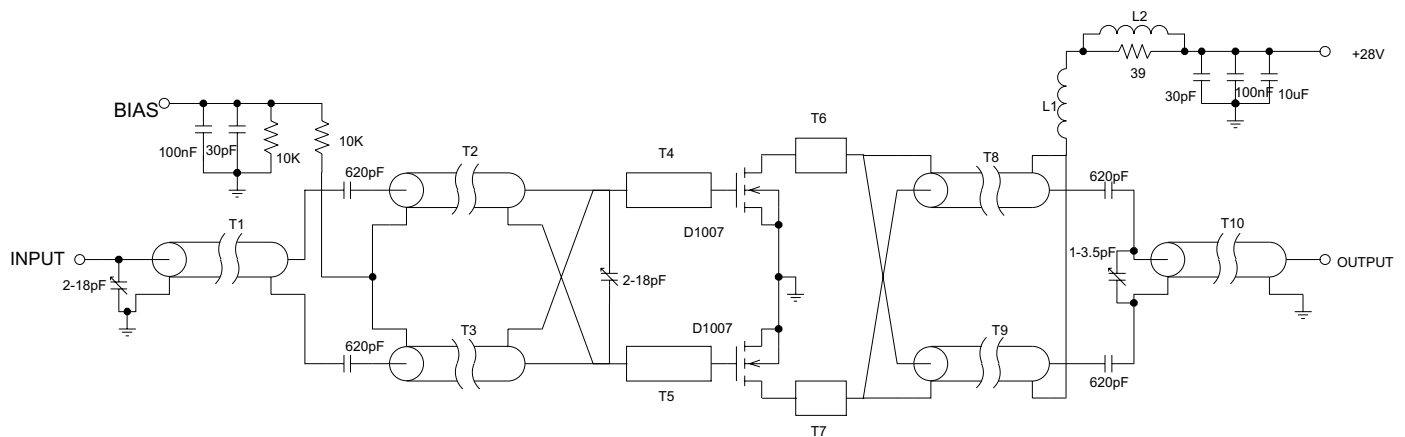
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z _S Ω	Z _L Ω
400MHz	10.7 - j35.4	13.8 - j22.2

Typical S Parameters

! V_{DS} = 28V, I_{DQ} = 1A
MHz S M A R 50

!Freq !MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
100	0.767	-135	22.646	88	0.0155	9	0.531	-103
200	0.813	-153	10.116	57	0.0099	4	0.692	-131
300	0.841	-161	5.623	39	0.0076	49	0.794	-143
400	0.861	-169	3.548	25	0.013	79	0.841	-151
500	0.882	-175	2.82	20	0.021	78	0.875	-156
600	0.902	180	2.093	14	0.0285	78	0.91	-161
700	0.923	174	1.365	9	0.0376	77	0.944	-166
800	0.912	170	1.096	2	0.0457	66	0.944	-170
900	0.923	164	0.902	-3	0.0484	66	0.933	-176
1000	0.923	161	0.724	-4	0.0596	64	0.944	-177



D1007 TEST FIXTURE

Substrate 1.6mm FR4

All microstrip lines $W = 2.5\text{mm}$

T1	45mm 50 OHM UT34 semi-rigid coax
T2, T3	55mm 50 OHM UT 34 semi-rigid coax
T4, T5	25mm microstrip line
T6, T7	10mm microstrip line
T8, T9	45mm 25 OHM UT 34-25 semi-rigid coax
T10	60mm 50OHM UT34 semi-rigid coax
L1	4 turns 19swg enamelled copper wire, 7mm i.d.
L2	2.5 turns of 19swg enamelled copper wire on T50-6 ferrite toroid

*D1007 (per side)

*PSPICE MODEL FOR POINT NINE TECHNOLOGIES, Inc RF N-CHANNEL VERTICAL DMOS POWER FET
*PRELIMINARY DATA, SEPTEMBER 1995

*THIS IS A PUSH-PULL DEVICE, MODEL DATA IS PER SIDE
*TO GENERATE S PARAMETERS MATCHING DATA SHEET, SET VG=3.7V FOR IDQ=1A

```
*      ____GATE
*      I      ____DRAIN
*      I      I      ____SOURCE
*      I      I      I
.SUBCKT D1007 10 20 30
LG 10 11 1.71N
RGATE 11 12 0.78
CG 10 30 0.05P
CRSS 12 17 2.5P
CISS 12 14 60P
LS 14 30 0.30N
CS 14 30 0.1P
LD 17 20 0.85N
CD 20 30 1.44P
R_RC 16 17 35.73
C_RC 14 16 11.8P
MOS 13 12 14 15 D1007MOS L=0.71U W=0.56332 ;D G S B LEVEL1
JFET 17 14 13 D1007JF ;D G S
DBODY 14 17 D1007DB ;P N

.MODEL D1007MOS NMOS (VTO=2.2 KP=1.8E-5 LAMBDA=0.1 RD=0.25 RS=0.5)
.MODEL D1007JF NJF (VTO=-7.5 BETA=0.04 LAMBDA=1)
.MODEL D1007DB D (CJO=88.5P RS=0.25 VJ=0.7 M=0.33 BV=70)
.ENDS
```

D1007.s2p (each side)

```
!      Vds=28V, Idq=1A
#      MHz S MA R 50
```

!Freq	S11		S21		S12		S22	
!MHz	mag	ang	mag	ang	mag	ang	mag	ang
100	0.767	-135	22.646	88	0.0155	9	0.531	-103
200	0.813	-153	10.116	57	0.0099	4	0.692	-131
300	0.841	-161	5.623	39	0.0076	49	0.794	-143
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800	0.912	170	1.096	2	0.0457	66	0.944	-170
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