POINT NINE
Technologies, Inc.

D1004

80W - 28V - 175MHz
GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET

FEATURES

- **METAL GATE**
- **EXTRA LOW Crss**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

APPLICATIONS

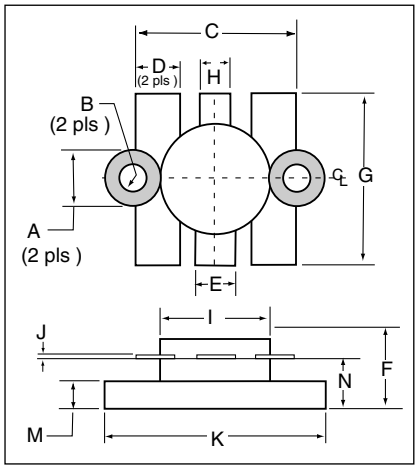
- **HF/VHF/UHF COMMUNICATIONS**

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C unless otherwise stated)		
P_D	Power Dissipation	175W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	±20V
I_D	Drain Current	20A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj\text{-}case}$	Thermal resistance junction-case	Max.1.0°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source	V_{GS}=0 I_D=100mA	70			Vdc
I_{DSS}	Drain leakage current	V_{DS}=28V V_{GS}=0			4	mAdc
I_{GSS}	Gate leakage current	V_{GS}=20V V_{DS}=0			1	µAdc
$V_{GS(th)}$	Gate threshold voltage	I_D=10mA V_{DS}=V_{GS}	1		7	Vdc
gfs	Transconductance (300µs pulse)	V_{DS}=10V I_D=4A	3.2			mhos
G_{PS}	Common source power gain	P_O=80W	16			dB
η	Drain efficiency	V_{DS}=28V I_{DQ}=0.8A	50			%
VSWR	Load mismatch tolerance	f=175MHz	20:1			
C_{iss}	Input capacitance	V_{DS}=0V V_{GS}=-5V f=1MHz			240	pF
C_{oss}	Output capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			120	pF
C_{rss}	Reverse transfer capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			10	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	6.35 DIA	.13	.250 DIA	.005
B	3.17 DIA	.13	.125 DIA	.005
C	18.41	.13	.725	.001
D	5.45	.13	.215	.005
E	5.21	.13	..205	.005
F	7.62	MAX	.300	MAX
G	21.59	.38	.850	.015
H	3.94	.13	.155	.005
I	4.32	.13	.170	.005
J	0.13	.02	.005	.001
K	24.76	.13	.975	.005
M	2.59	.13	.095	.005
N	4.06	.25	.170	.010

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

2697 Lavery Court #8 • Newbury Park, CA 91320 • (805) 375-6600 • Fax: (805) 375-6602 • www.point9.com • www.rfmosfet.com

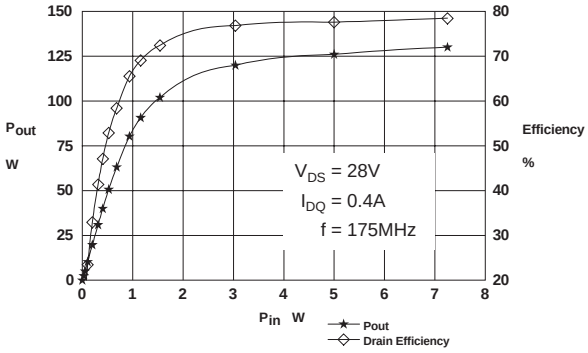


Figure 1 – Power Output and Efficiency vs. Power Input.

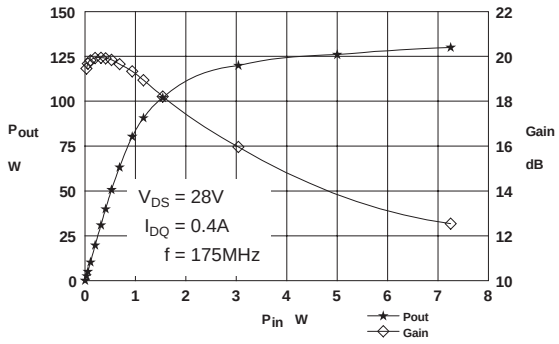


Figure 2 – Power Output & Gain vs. Power Input.

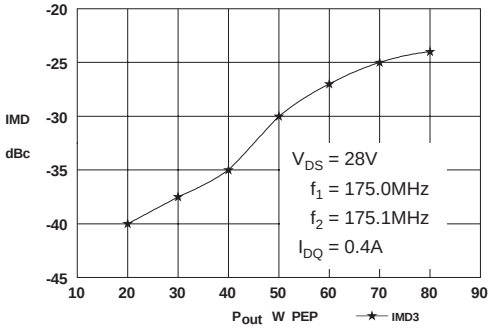
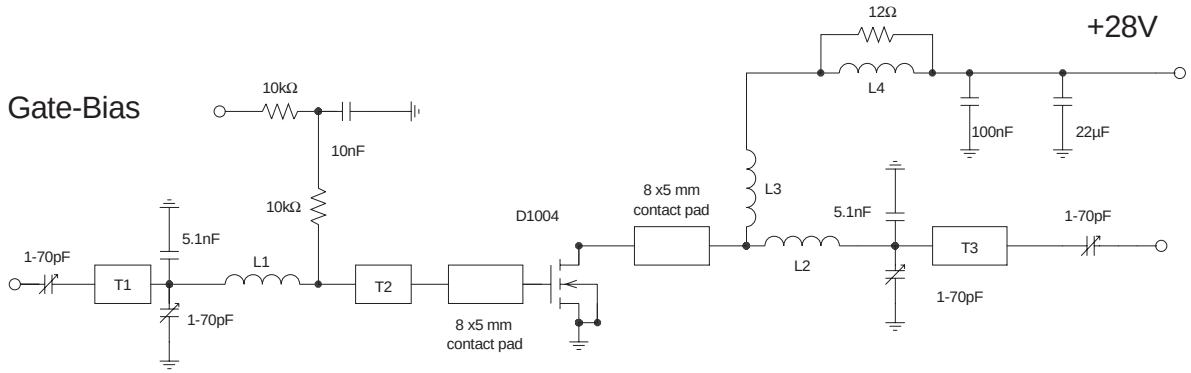


Figure 3 – IMD vs. Output Power.

D1004
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175MHz	2.2 + j1.9	3.2 - j0.5



D1004 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/ glass, Er= 2.5
All microstrip lines W=4.4mm

T1 7.5mm
T2 6mm
T3 8mm

L1 Hairpin loop 16swg 13mm dia
L2 Hairpin loop 16swg 11mm dia
L3 10 turns 18swg enamelled copper wire, 4mm i.d.
L4 12 turns 18swg enamelled copper wire on 22.7mm o.d. ferrite core

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*D1004

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I    ____SOURCE
*                  I   I   I
.SUBCKT D1004  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1  10    30    0.32p
Lin   10    11    0.59n
Cin2  11    30    0.32p
LG    11    12    2n      ;Gate bond wire inductance
CGS   12    13    184p    ;Gate-source capacitance
MOS   14    12    13     13  D1004 L=0.9U W=0.224    ;D G S B LEVEL1
JFET  16    13    14     D1004                       ;D G S
DBODY 13    16           D1004                       ;P N
LS    13    30    0.3n    ;Source bond wire inductance
CGD   12    16    4p      ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1   16    30    1.05p
Lout    16    20    1.77n
Cout2   20    30    1.05p

.MODEL D1004 NMOS (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.019 RS=0.077)
.MODEL D1004  NJF  (VTO=-4.3 BETA=1 LAMBDA=0.54)
.MODEL D1004  D    (CJO=328.8P RS=0.25 VJ=0.7 M=0.35 BV=75)


.ENDS
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