POINT NINE
Technologies, Inc.

D1002

40W - 28V - 175MHz
GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET

FEATURES

- **METAL GATE**
- **EXTRA LOW Crss**
- **BROAD BAND**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN**

APPLICATIONS

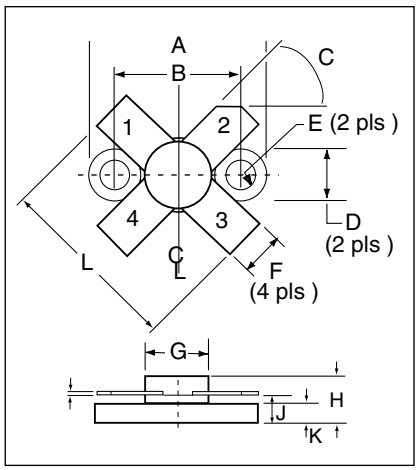
- **HF/VHF/UHF COMMUNICATIONS**

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C unless otherwise stated)		
P_D	Power Dissipation	87W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	±20V
I_D	Drain Current	10A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj\text{-}case}$	Thermal resistance junction-case	Max.2.0°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source	V_{GS}=0 I_D=100mA	70			Vdc
I_{DSS}	Drain leakage current	V_{DS}=28V V_{GS}=0			2	mAdc
I_{GSS}	Gate leakage current	V_{GS}=20V V_{DS}=0			1	µAdc
$V_{GS(th)}$	Gate threshold voltage	I_D=10mA V_{DS}=V_{GS}	1		7	Vdc
gfs	Transconductance (300µs pulse)	V_{DS}=10V I_D=2A	1.6			mhos
G_{PS}	Common source power gain	P_O=40W	16			dB
η	Drain efficiency	V_{DS}=28V I_{DQ}=0.8A	50			%
VSWR	Load mismatch tolerance	f=175MHz	20:1			
C_{iss}	Input capacitance	V_{DS}=0V V_{GS}=-5V f=1MHz			120	pF
C_{oss}	Output capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			60	pF
C_{rss}	Reverse transfer capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	24.76	.13	.975	.005
B	18.42	.13	.725	.005
C	45°	5°	45°	5°
D	6.35	.13	.250	.005
E	3.17 DIA	.13	.125 DIA	.005
F	5.71	.13	.225	.005
G	9.52 DIA	.13	.375 DIA	.005
H	6.60	REF	.260	REF
I	.13	.02	.005	.001
J	4.32	.13	.170	.005
K	2.54	.13	.100	.005
L	20.32	.25	.800	.010

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

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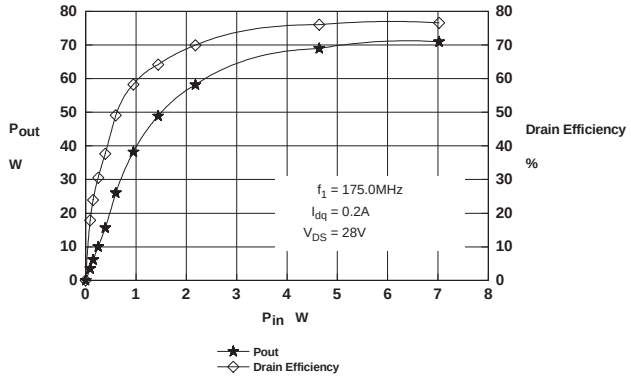

Figure 1 – Power Output and Efficiency vs. Power Input.

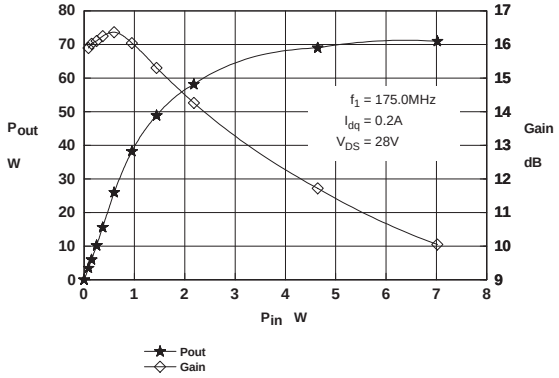

Figure 2 – Power Output & Gain vs. Power Input.

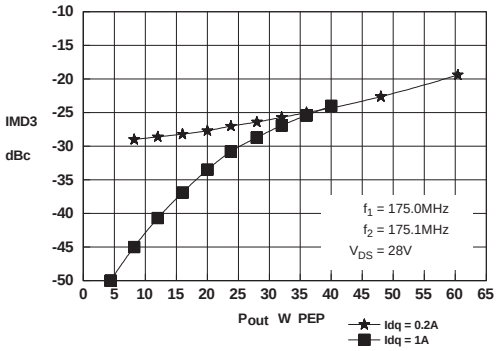

Figure 3 – IMD vs. Output Power.

D1002
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175MHz	3.8 + j6.5	4.6 + j0.4

Typical S Parameters

! Vds=28V Idq=0.2A
MHZ S MA R 50

!Freq MHz	S11 mag	S11 ang	S21 mag	S21 ang	S12 mag	S12 ang	S22 mag	S22 ang
50	0.76	-144	15.6	86	0.026	1	0.58	-119
100	0.79	-155	7.1	61	0.021	-9	0.66	-132
150	0.84	-163	4.2	43	0.012	-3	0.74	-144
200	0.87	-169	2.7	33	0.009	47	0.81	-154
250	0.90	-176	1.9	23	0.016	76	0.85	-163
300	0.92	177	1.5	20	0.025	87	0.88	-172
350	0.94	170	1.1	11	0.033	85	0.91	-180
400	0.96	163	0.9	6	0.046	82	0.94	172
450	0.97	156	0.7	-2	0.051	78	0.96	165
500	0.98	150	0.6	-8	0.062	76	0.98	157
550	0.98	144	0.4	-12	0.068	74	0.98	152
600	0.98	141	0.4	-14	0.078	67	0.98	148

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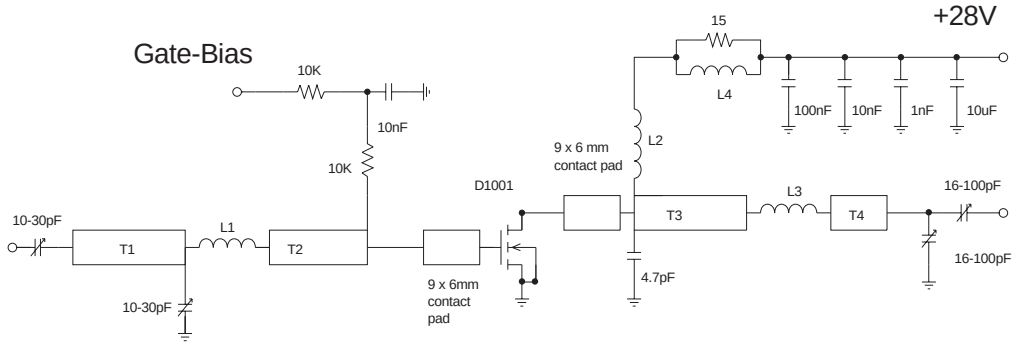

D1002 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/glass, Er=2.5
All microstrip lines W=4.4mm

T1	10mm
T2	13mm
T3	12mm
T4	4mm

L1	1.5 turns 22swg enamelled copper wire, 6mm i.d.
L2	10 turns 19swg enamelled copper wire, 6mm i.d.
L3	1.5 turns 22swg enamelled copper wire, 6mm i.d.
L4	13.5 turns 19swg enamelled copper wire on Siemens B64920A618X830 ferrite core

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*D1002

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1002  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.31p
Lin    10    11    0.64n
Cin2   11    30    0.24p
LG     11    12    1n    ;Gate bond wire inductance
CGS    12    13    92p   ;Gate-source capacitance
MOS    14    12    13     13  D1002 L=0.9U W=0.112    ;D G S B LEVEL1
JFET   16    13    14    D1002                        ;D G S
DBODY  13    16    D1002                              ;P N
LS     13    30    0.7n    ;Source bond wire inductance
CGD    12    16    2p    ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1   16    30    0.65p
Lout    16    20    1.5n
Cout2   20    30    0.6p

.MODEL D1002  NMOS  (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.038 RS=0.153)
.MODEL D1002  NJF  (VTO=-4.3 BETA=0.5 LAMBDA=0.54)
.MODEL D1002  D    (CJO=164.4P RS=0.25 VJ=0.7 M=0.35 BV=75)


.ENDS
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